

Docket No.: 60188-075

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :  
Makoto FUJIWARA :  
Serial No.: Group Art Unit:  
Filed: May 31, 2001 Examiner:  
For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING  
SEMICONDUCTOR INTEGRATED CIRCUIT

11002 U.S. PRO  
09/867766  
05/31/01



CLAIM OF PRIORITY

Commissioner for Patents  
Washington, DC 20231

Sir:

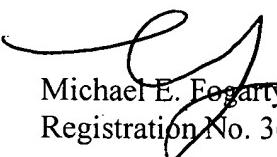
In accordance with the provisions of 35 U.S.C. 119, Applicant hereby claims the priority of:

Japanese Patent Application No. 2000-161343,  
Filed May 31, 2000

A certified copy will be filed in due course.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Michael E. Fogarty  
Registration No. 36,139

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
(202) 756-8000 MEF:ykg  
**Date: May 31, 2001**  
Facsimile: (202) 756-8087